oxide layer over and around the polysilicon region in a single step, which is in contact with said projecting region (2), and of a larger isolation layer, which method also includes a silicidation process to which the upper part of the polysilicon region is subjected, which silicidation process includes the deposition on said upper part of a metal layer which is capable of forming a metal silicide (5) with the silicon, characterized in that the silicidation process includes, prior to the deposition of said metal layer, an etch step to which at least the vertical portion of the smaller isolation layer (402) is subjected so as to form a trench (TR) between the larger isolation layer (411) of each lateral isolation region and the corresponding side (F) of the polysilicon region (2), wherein a depth of the trench, measured from a top of the larger isolation layer down to the smaller isolation layer, is maximally half the height of the larger isolation area, and in that the deposition of the metal layer is a directional deposition.

6. (TWICE AMENDED) An integrated circuit comprising lateral isolation regions formed at the sides of a least one projecting region of polysilicon so as to be in contact therewith, each lateral isolation region being composed of a smaller isolation layer (402), contacting said projecting region (2), and a larger isolation layer (411), and comprising a zone (5) including a metal silicide situated in the upper part of the polysilicon region (2), characterized in that each lateral isolation region comprises a vertical trench (TR) made in the smaller isolation layer (402) between the larger isolation layer (411) and the corresponding side (F) of the projecting region (2), said trench (TR) extending from the top of the larger isolation layer (411) of the corresponding lateral isolation region down